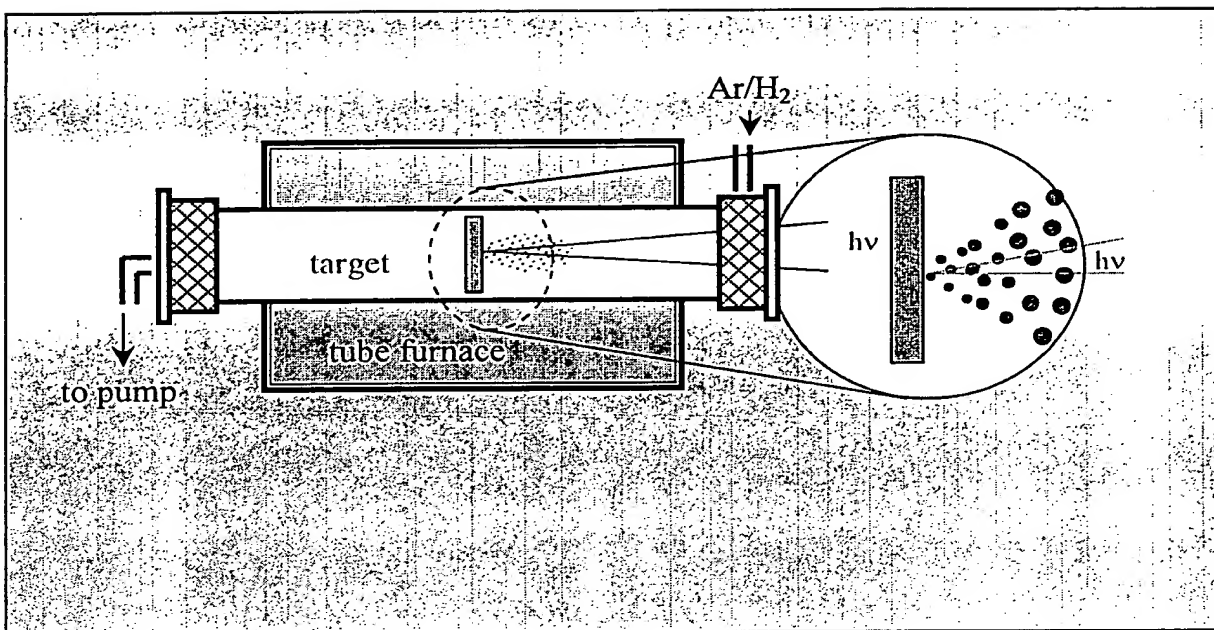
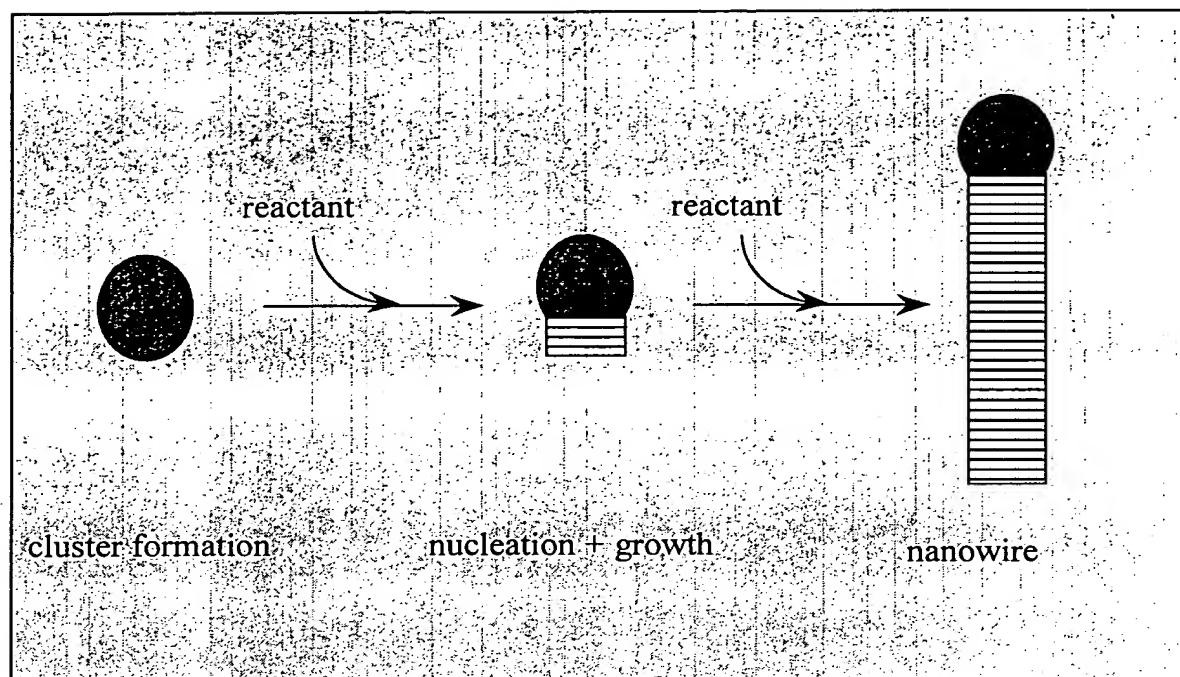
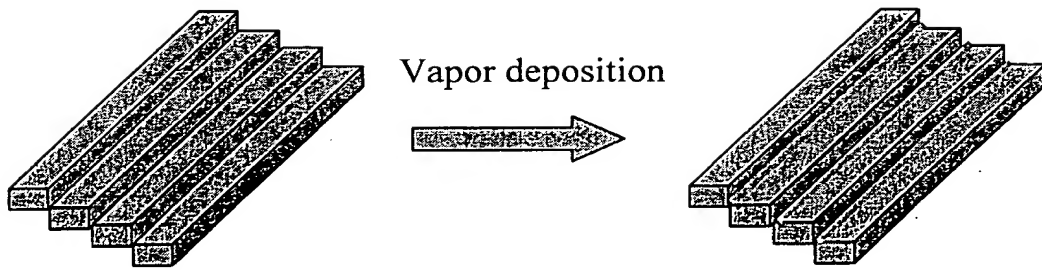


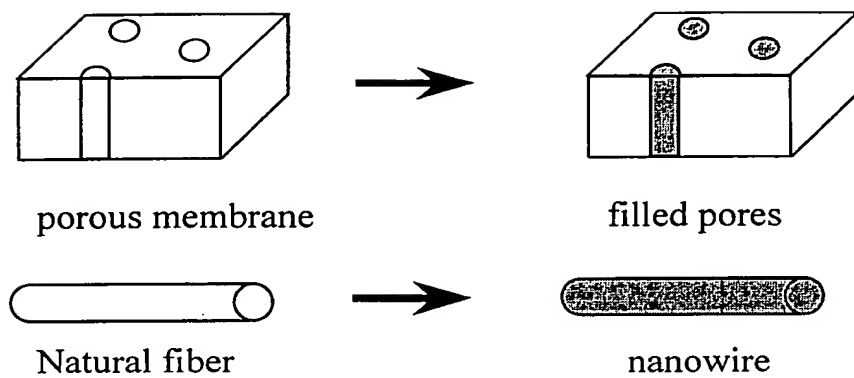
FIG. 1

**FIG. 2**

**FIG. 3**



**FIG. 5**

**FIG. 6**

# Orthogonal Assembly of Semiconductor Nanowires

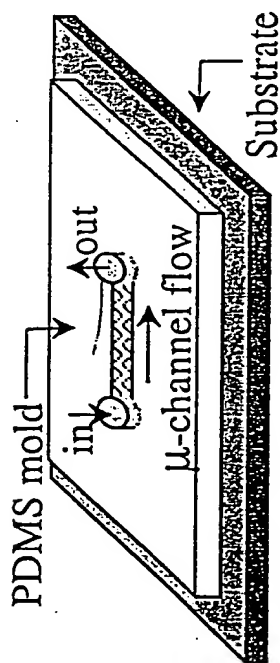


FIG. 7A

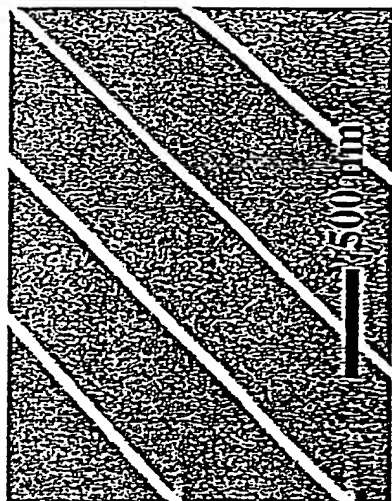
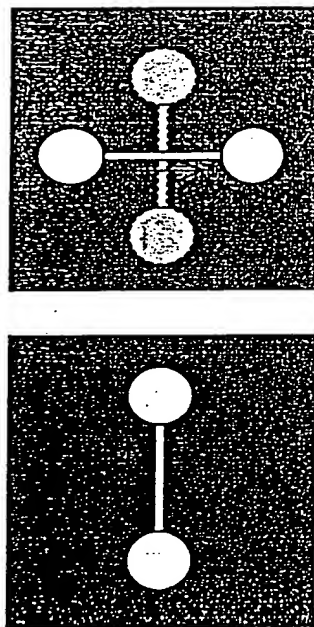


FIG. 7B



First layer

Second layer

FIG. 7C

FIG. 7D

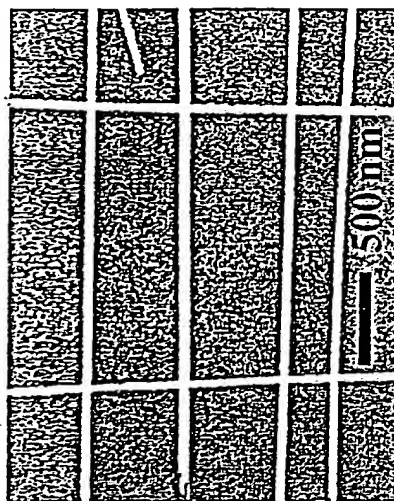


FIG. 7E

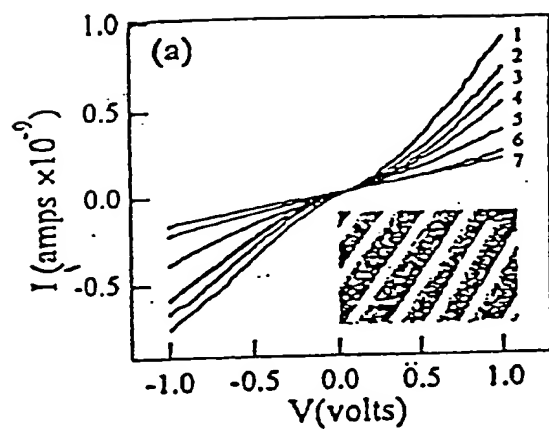


FIG. 8A

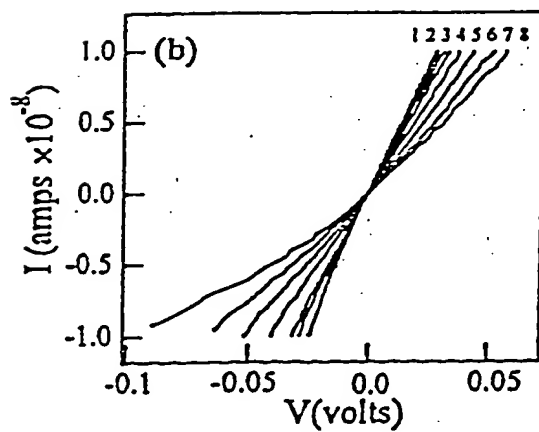


FIG. 8B

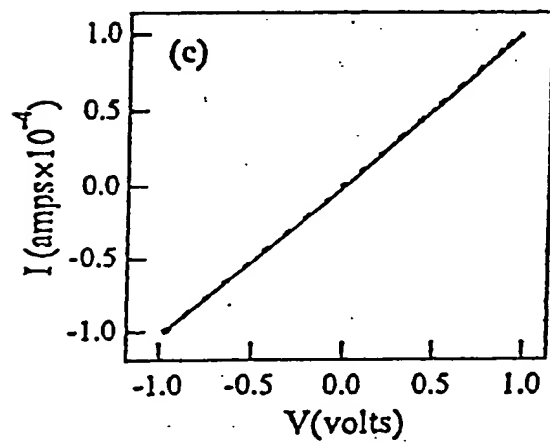
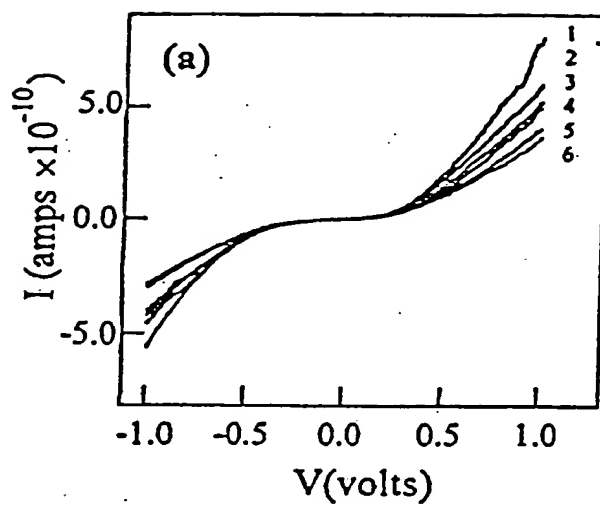
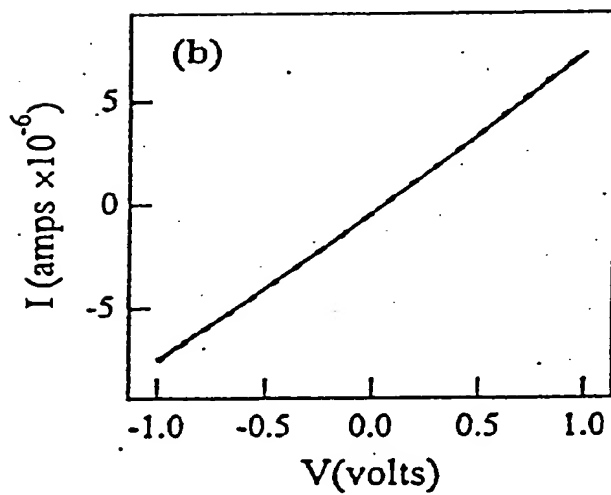


FIG. 8C



**FIG. 9A****FIG. 9B**

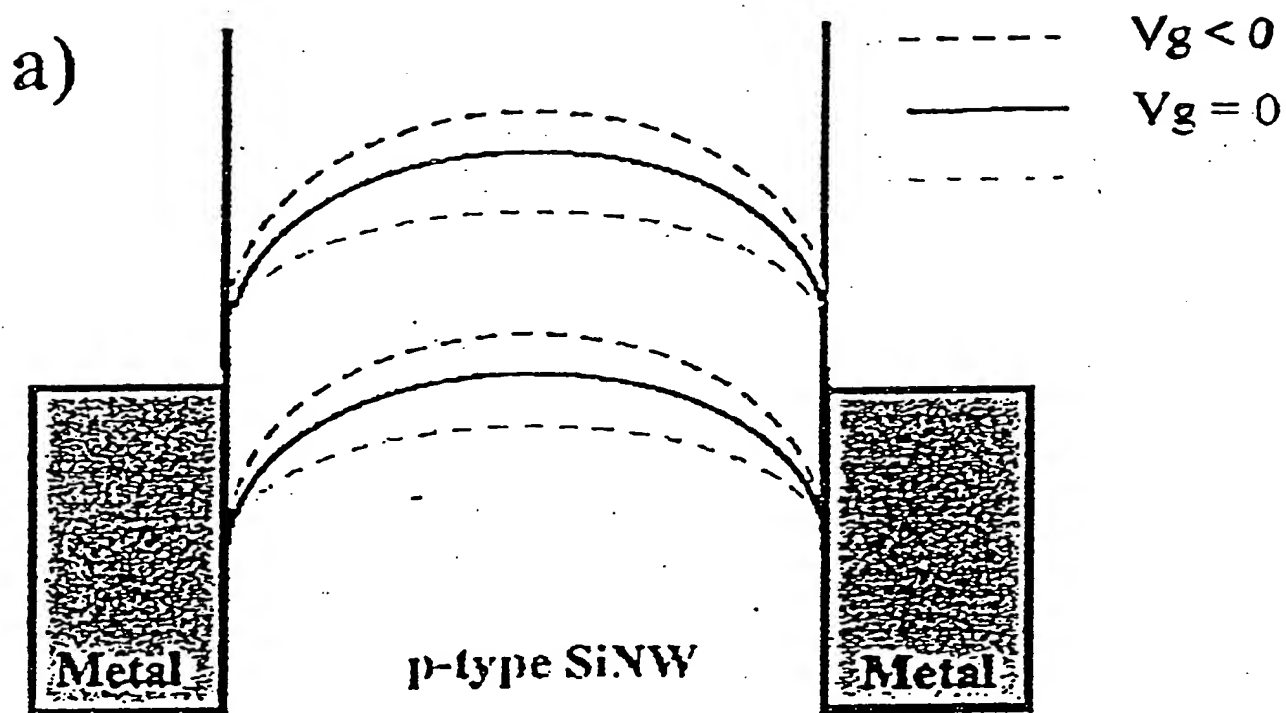


FIG. 10A

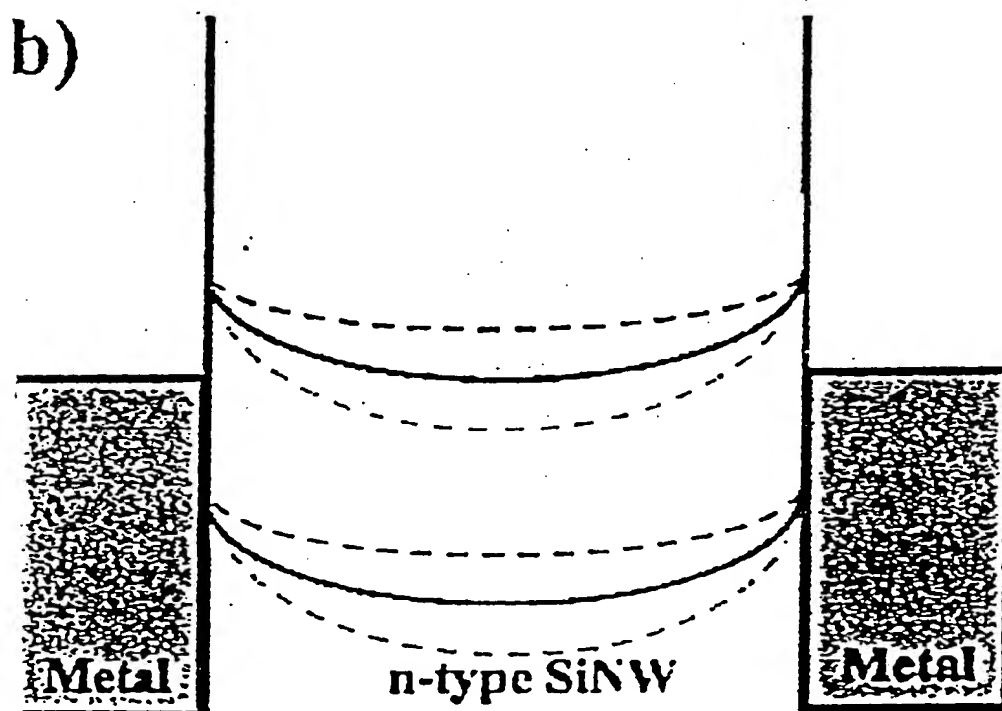
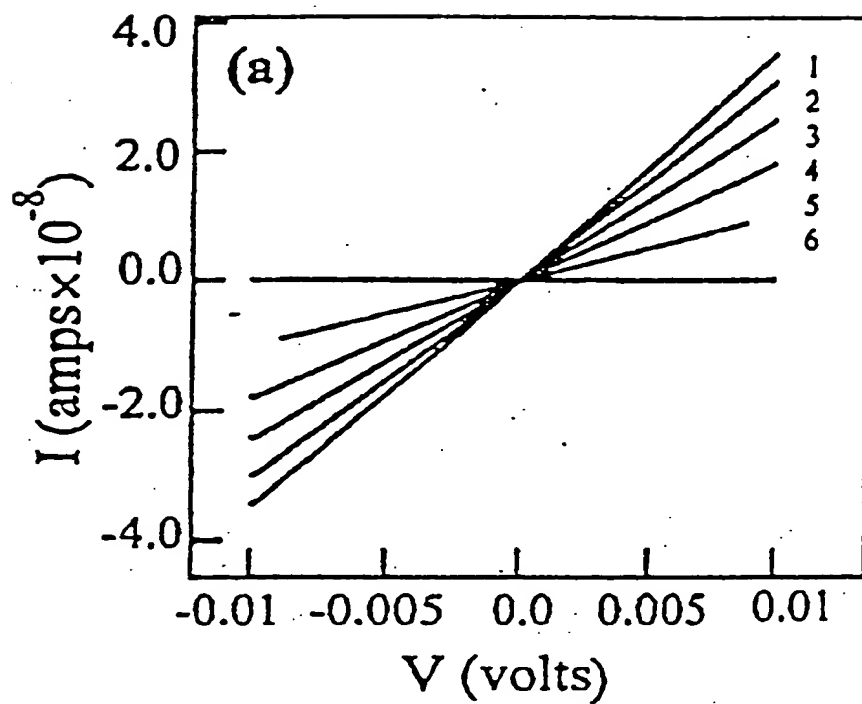
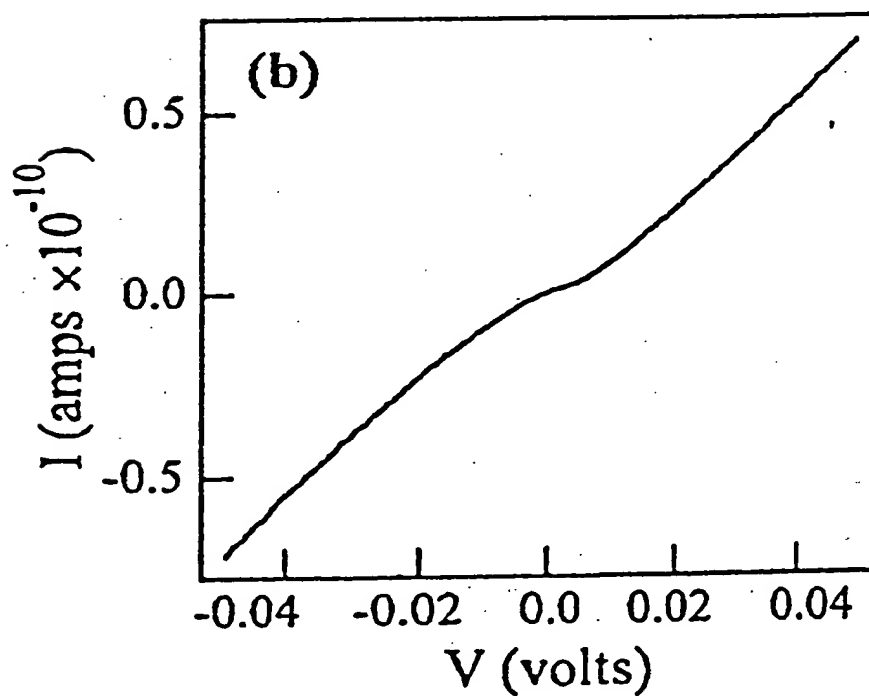
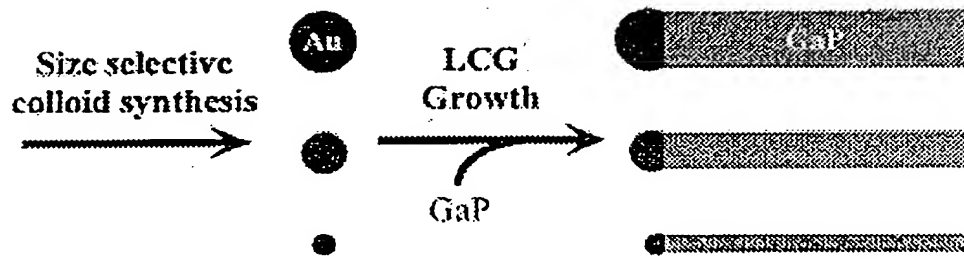


FIG. 10B

**FIG. 11A****FIG. 11B**

**FIG. 12**

FOUO 92252600

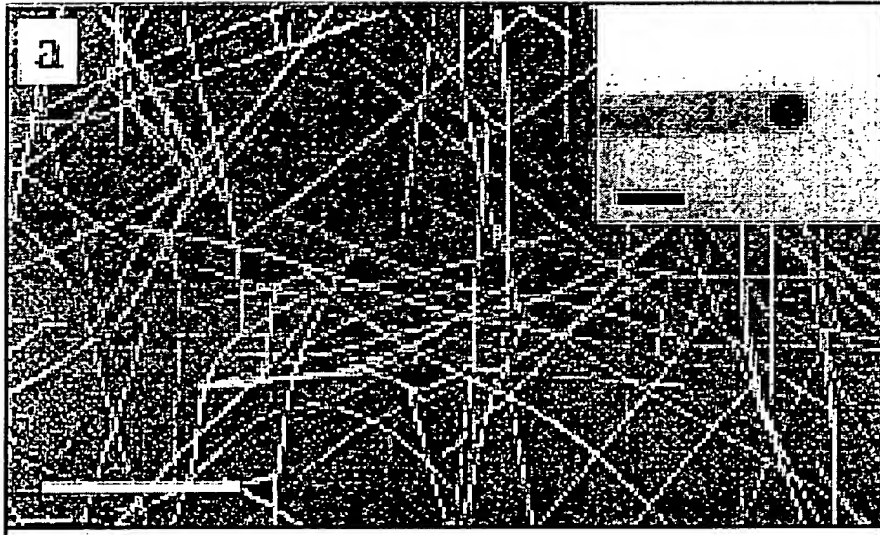


FIG. 13A

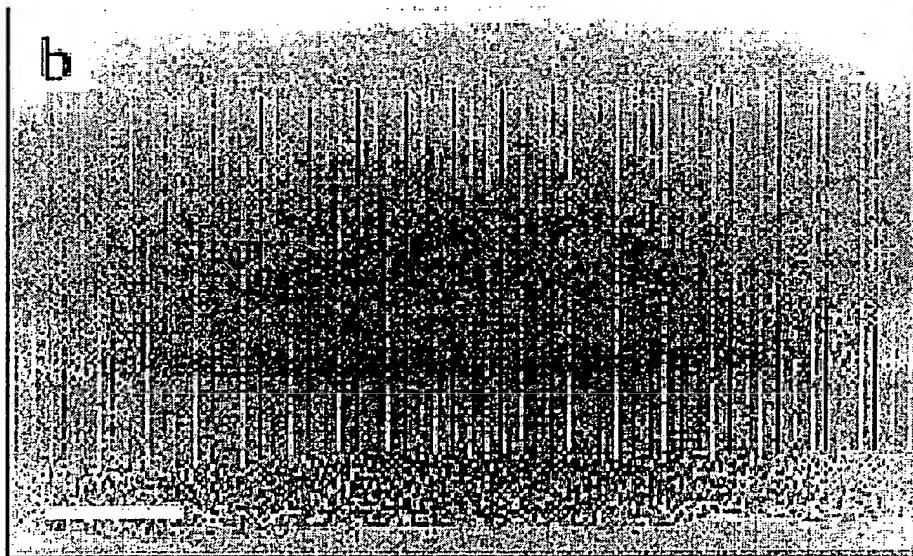


FIG. 13B

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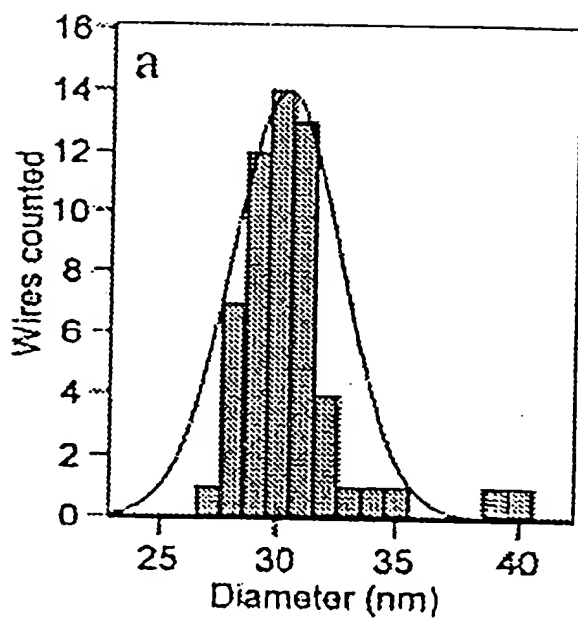


FIG. 14A

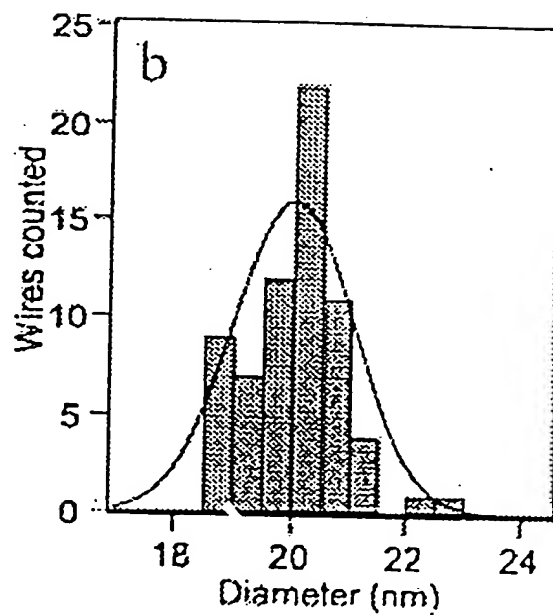


FIG. 14B

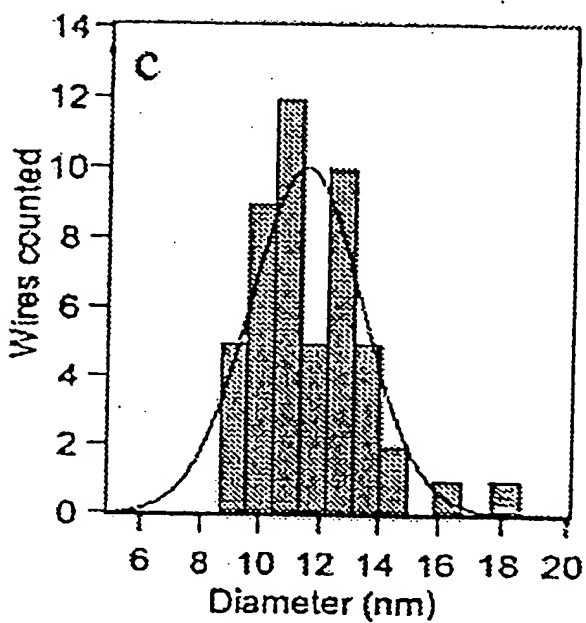


FIG. 14C

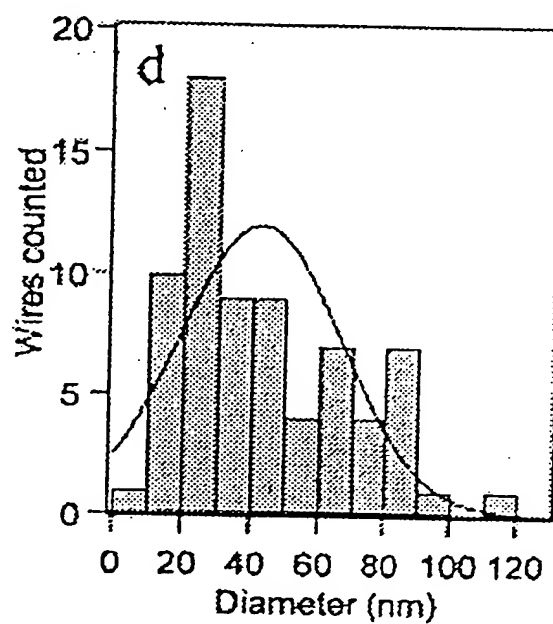


FIG. 14D

FOUO 3425000

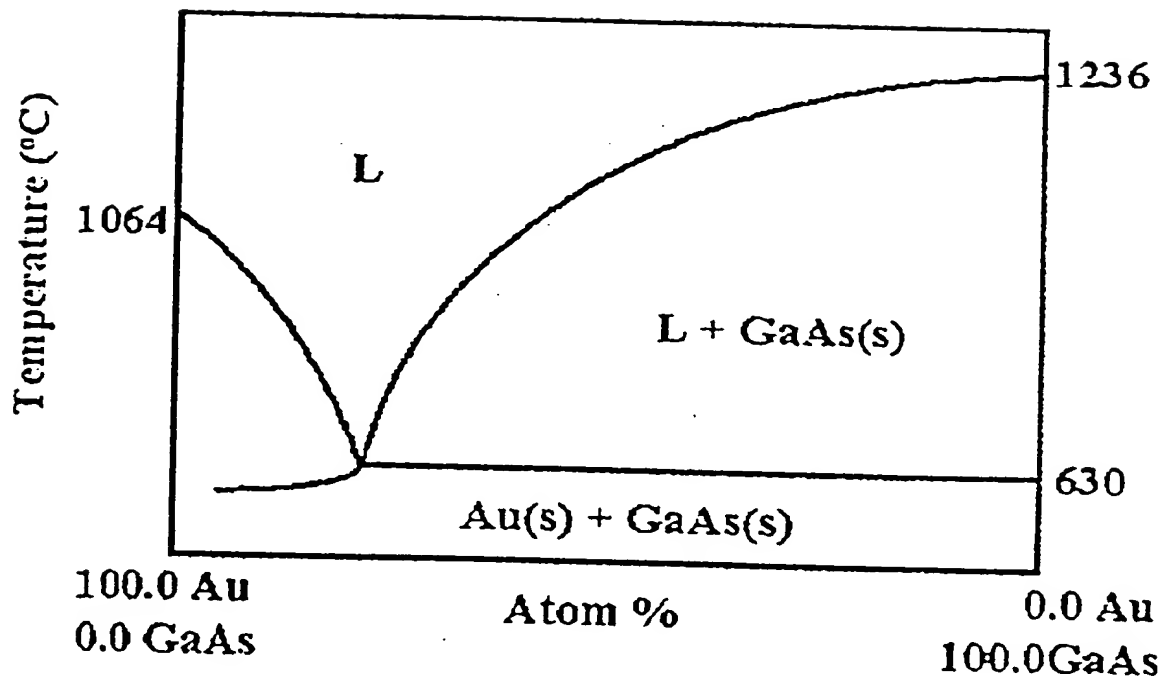


FIG. 15

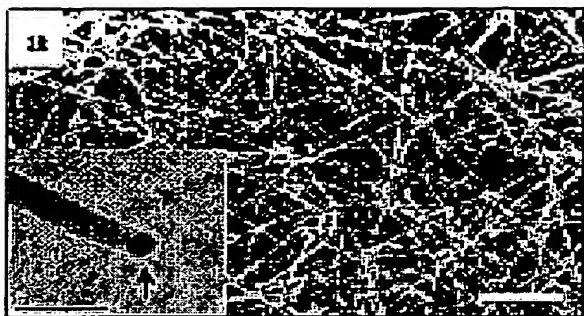


FIG. 16A

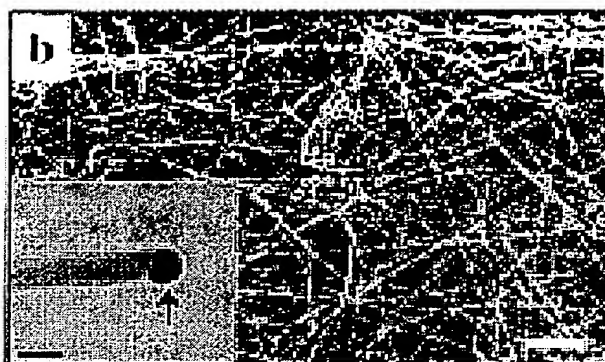


FIG. 16B

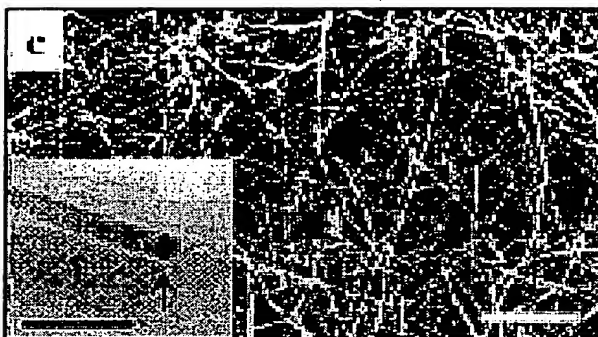
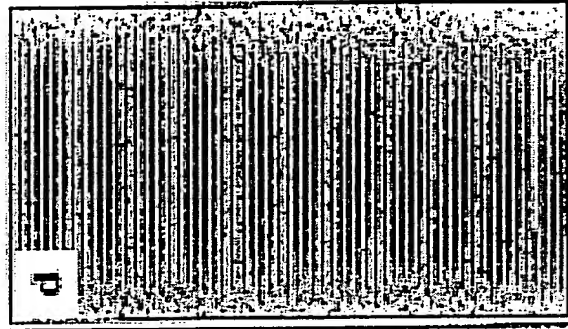
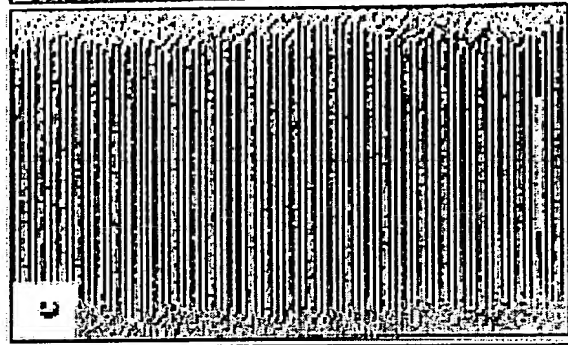
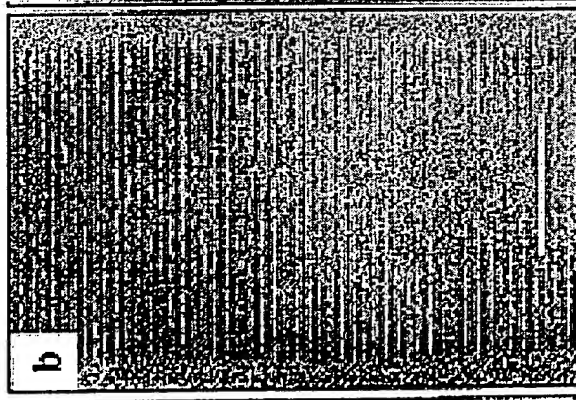
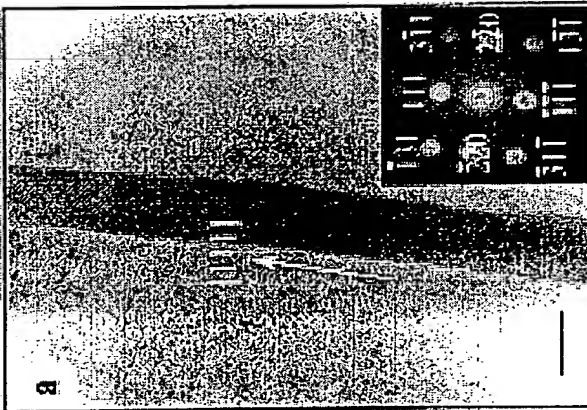


FIG. 16C

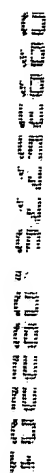
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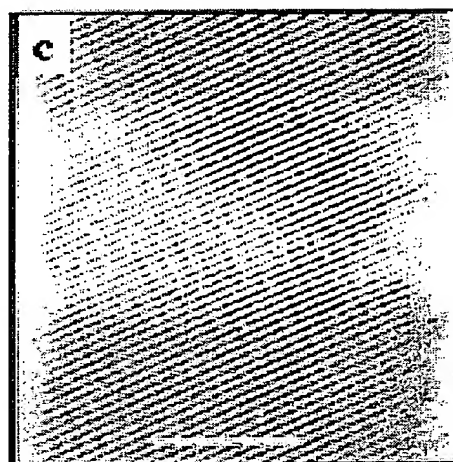
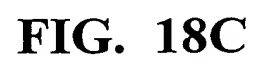




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**FIG. 18B**



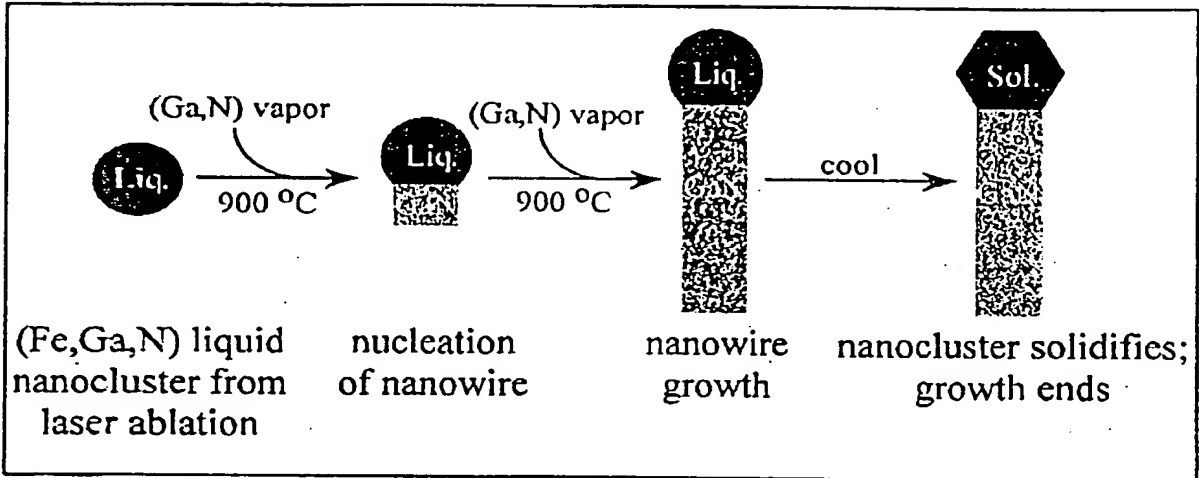
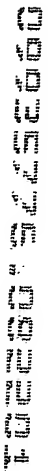
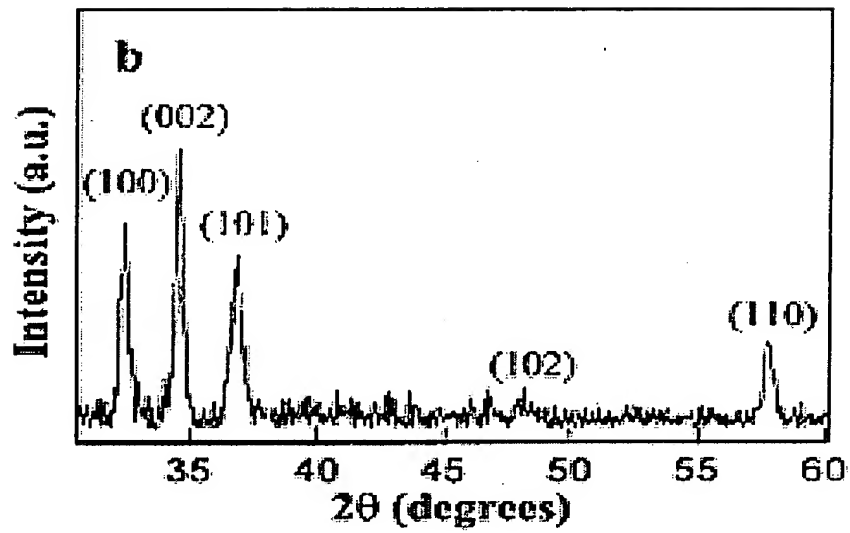
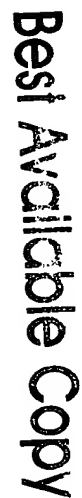


FIG. 19



**FIG. 20B**





**FIG. 21B**

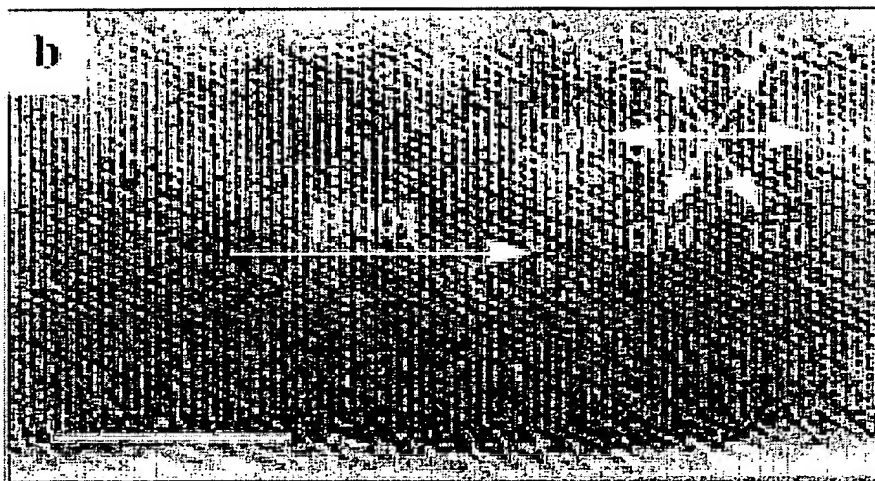




Figure 1 consists of a main plot and an inset. The main plot is a graph of Current ( $\mu\text{A}$ ) versus Voltage (V). The y-axis ranges from -8 to 8  $\mu\text{A}$  with major ticks at -8, -4, 0, 4, and 8. The x-axis ranges from -0.8 to 0.8 V with major ticks at -0.8, -0.4, 0.0, 0.4, and 0.8. Four curves are shown, corresponding to different gate voltages: -60 V, -30 V, 0 V, and +60 V. The curves are symmetric about the origin and show a non-linear, rectifying-like behavior. The inset is a micrograph of the device structure, showing a central region with a scale bar of 1  $\mu\text{m}$ .

**FIG. 22C**

FIG. 23A

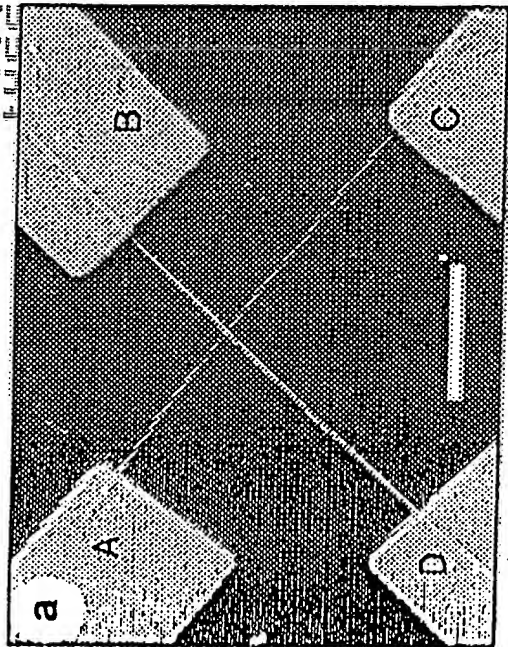


FIG. 23A

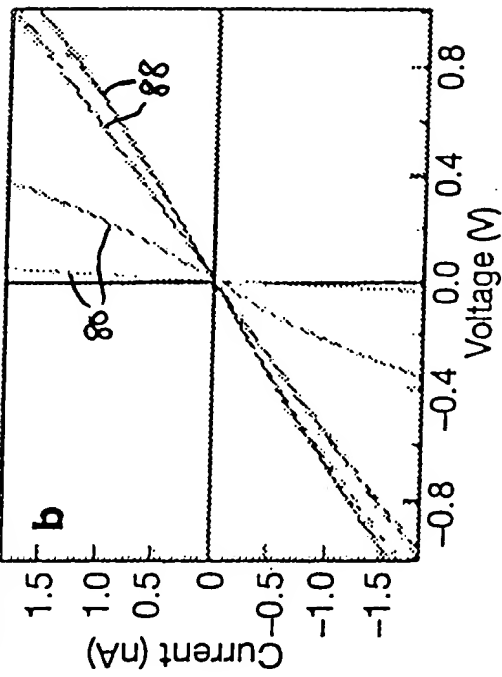


FIG. 23B

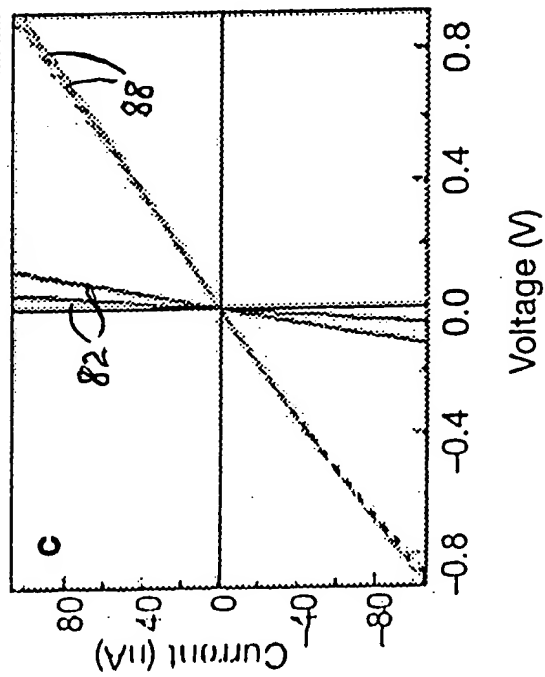


FIG. 23C

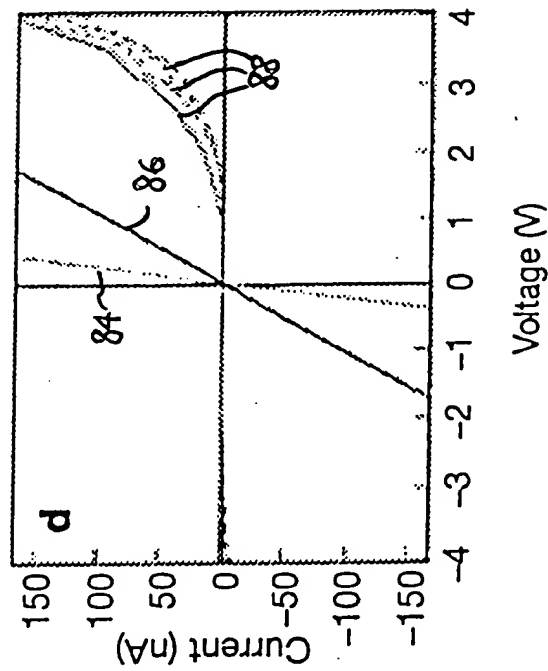
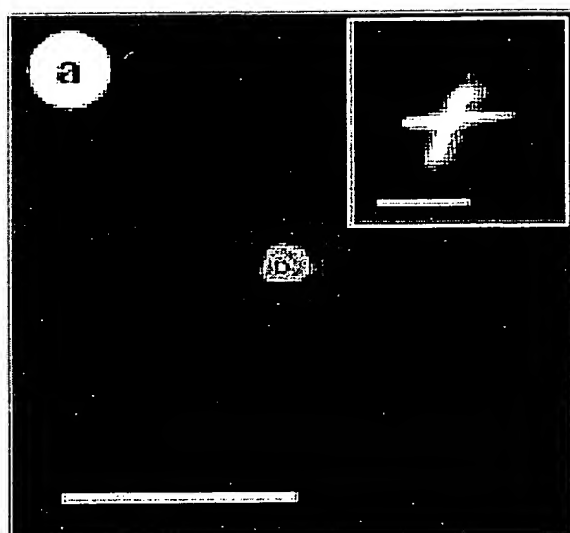
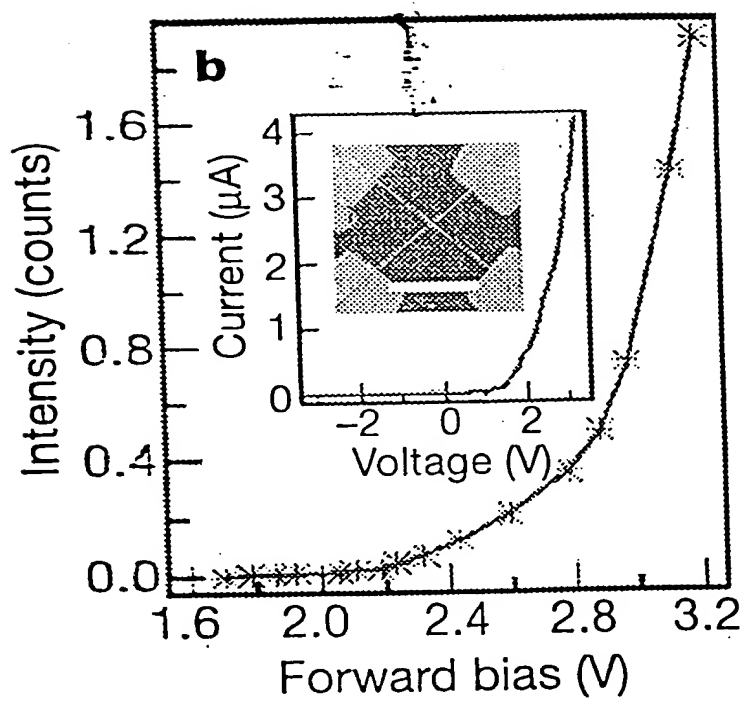


FIG. 23D

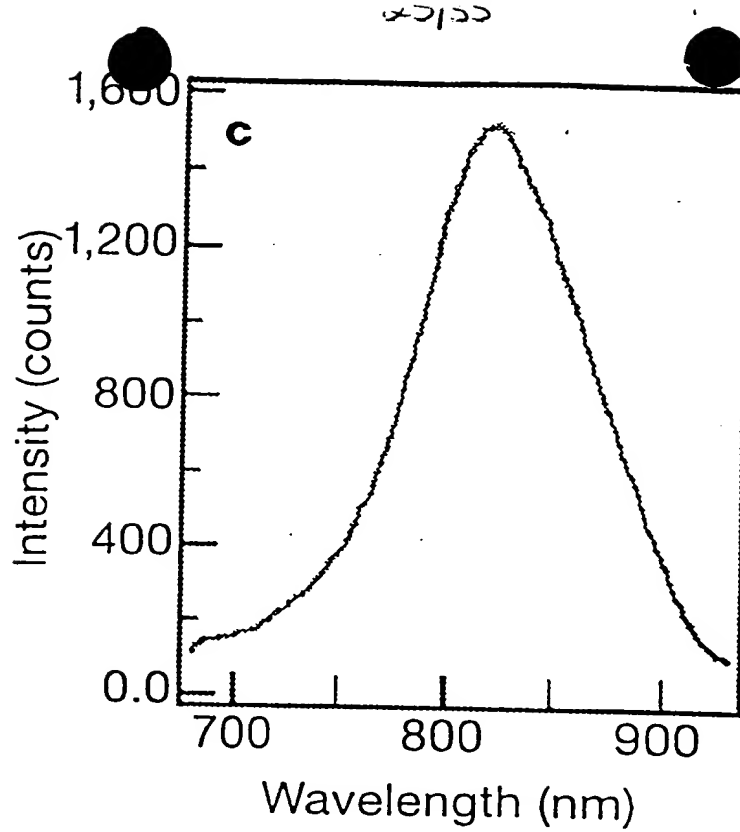


**FIG. 24A**

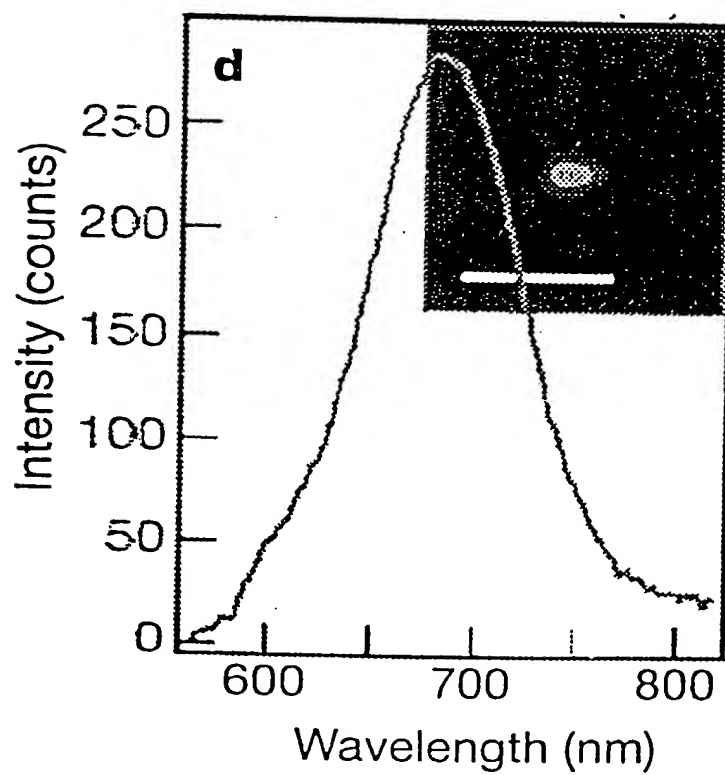


**FIG. 24B**





**FIG. 24C**

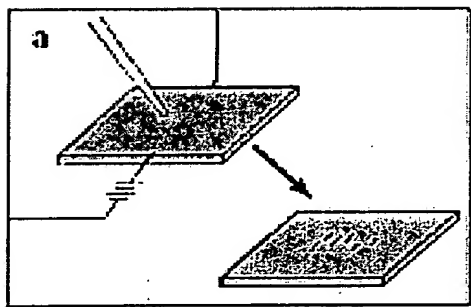


**FIG. 24D**

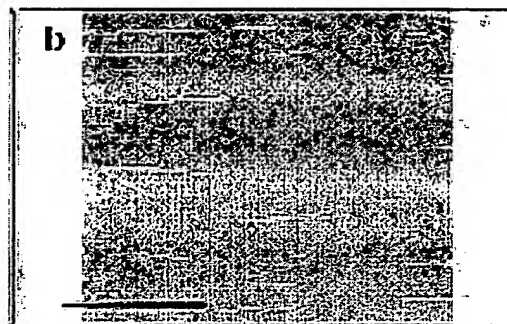
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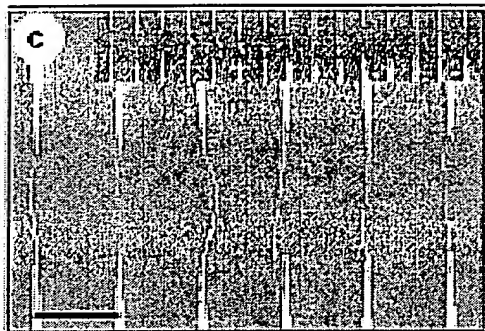




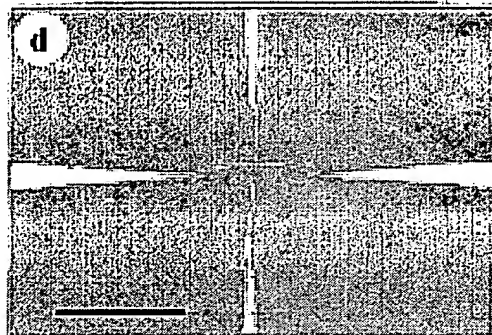
**FIG. 26A**







**FIG. 26B**










**FIG. 26A**









**FIG. 26B**









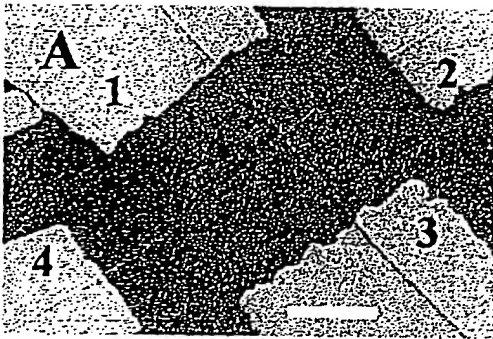



FIG. 27A

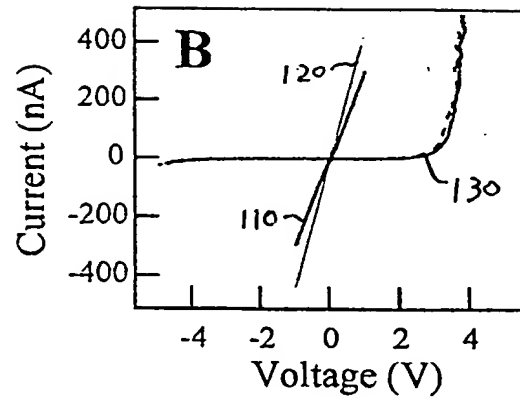


FIG. 27B

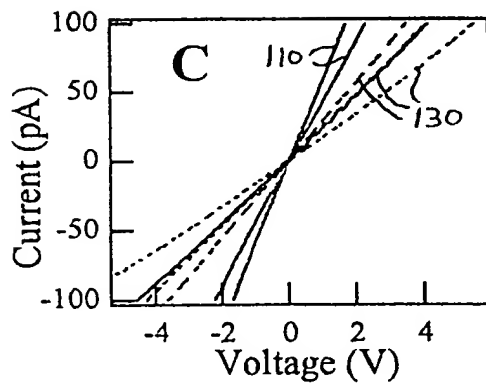


FIG. 27C

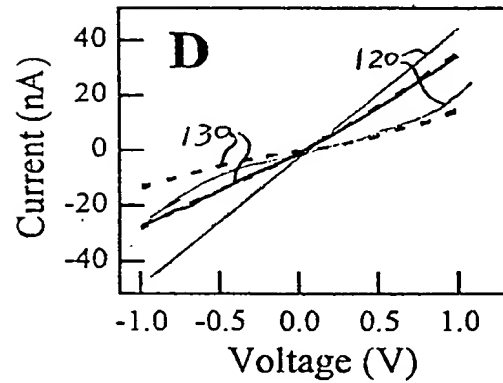
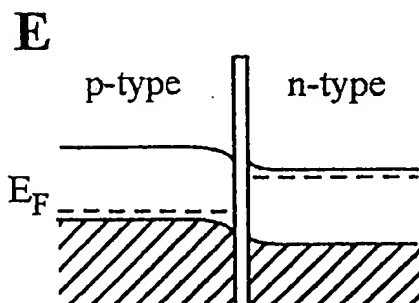
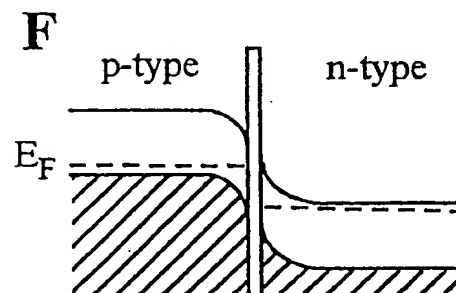


FIG. 27D



forward bias

FIG. 27E



reverse bias

FIG. 27F

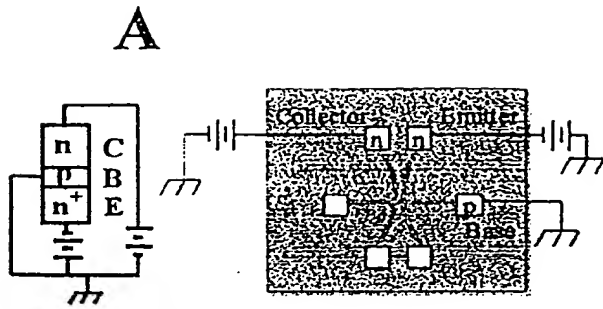


FIG. 28A

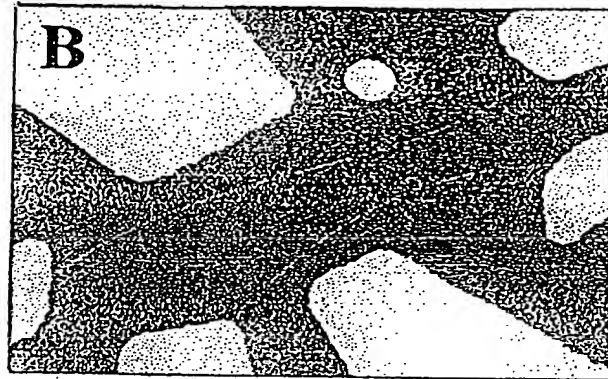


FIG. 28B

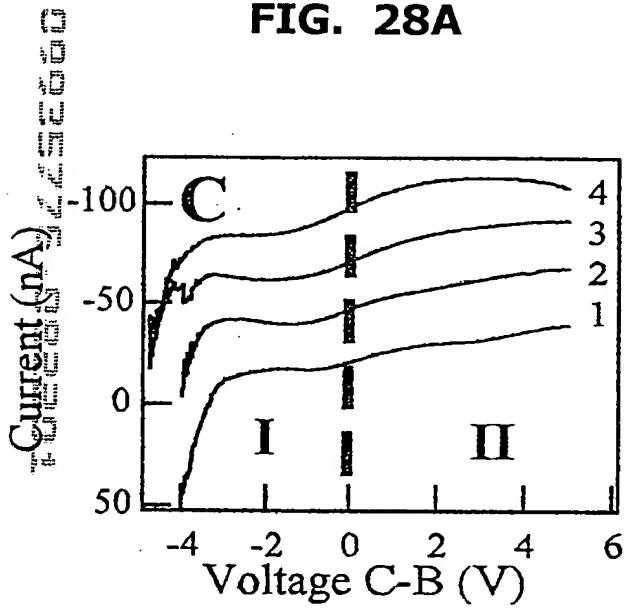


FIG. 28C

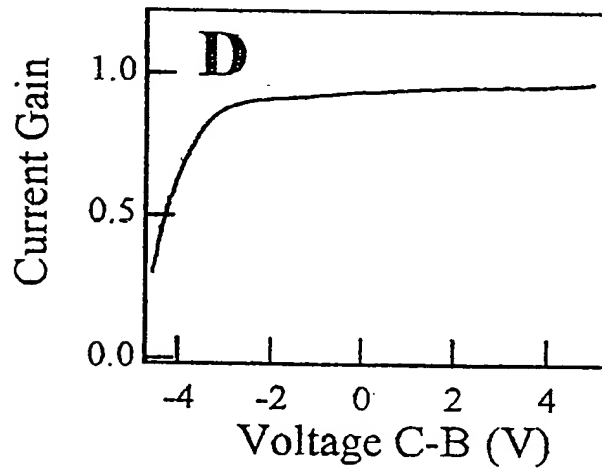


FIG. 28D

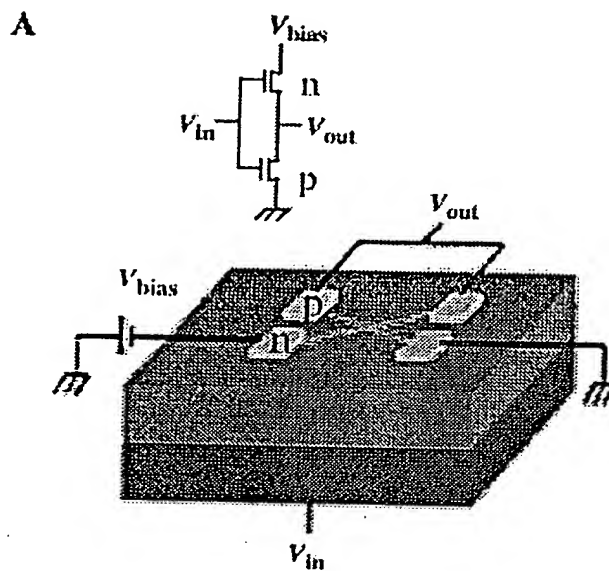


FIG. 29A

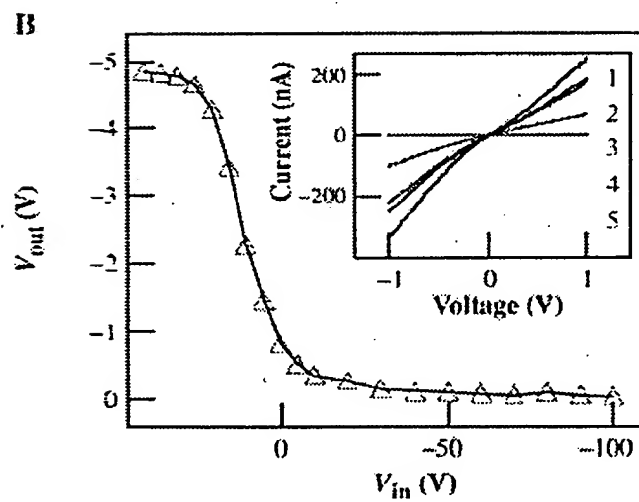


FIG. 29B

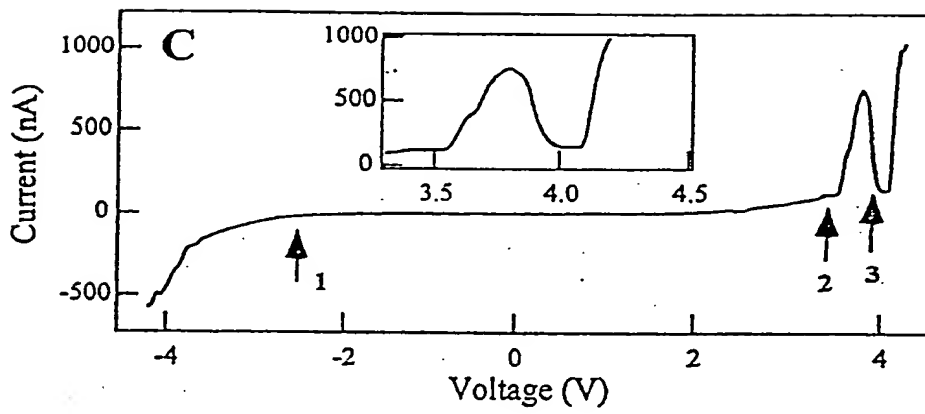


FIG. 29C

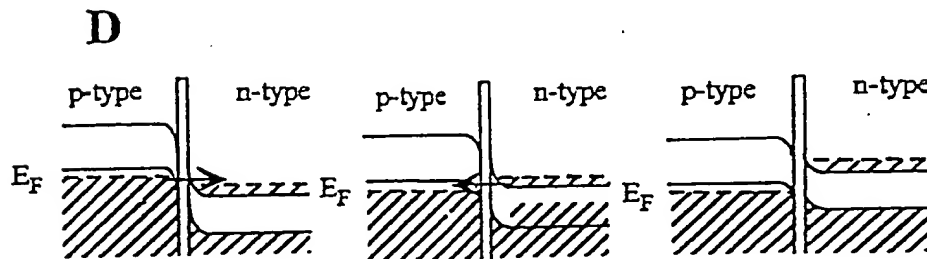


FIG. 29D

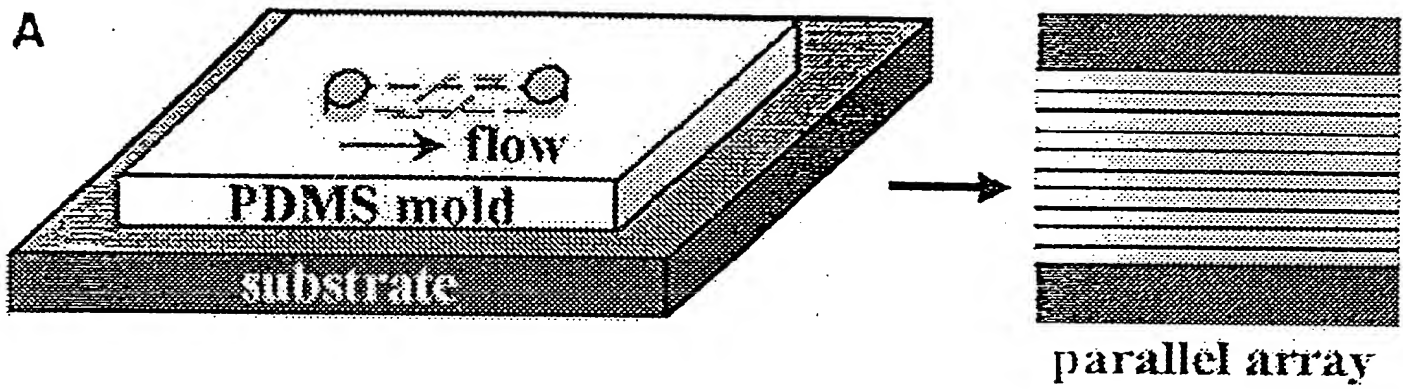


FIG. 30A

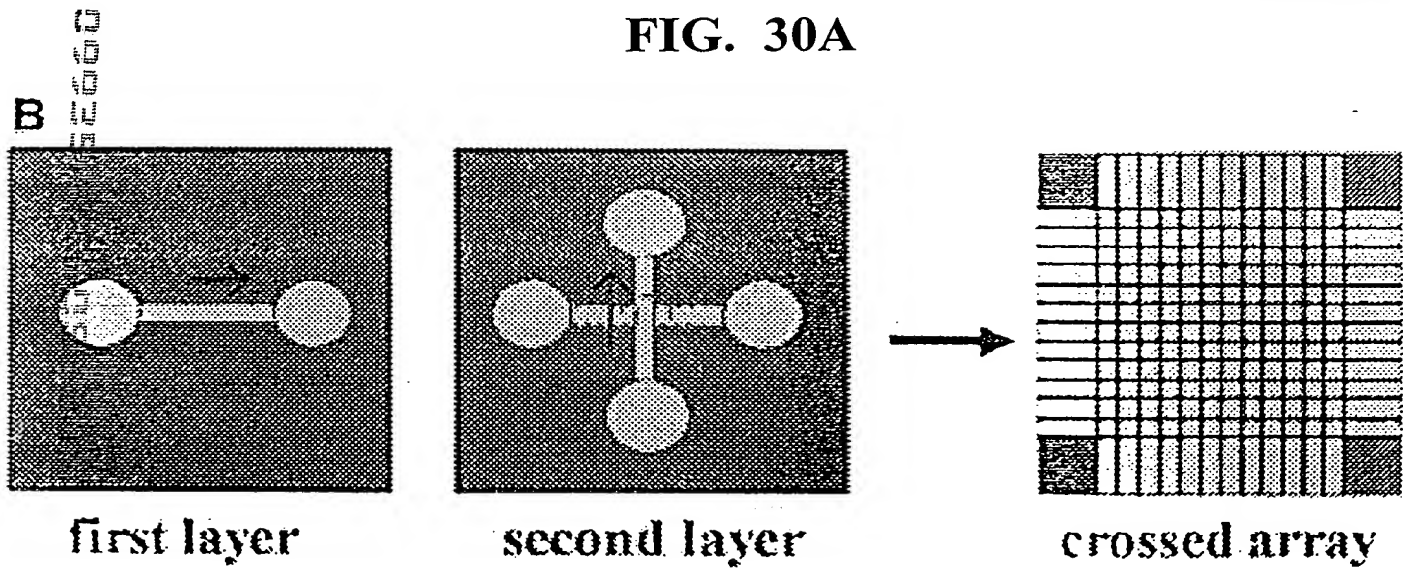


FIG. 30B



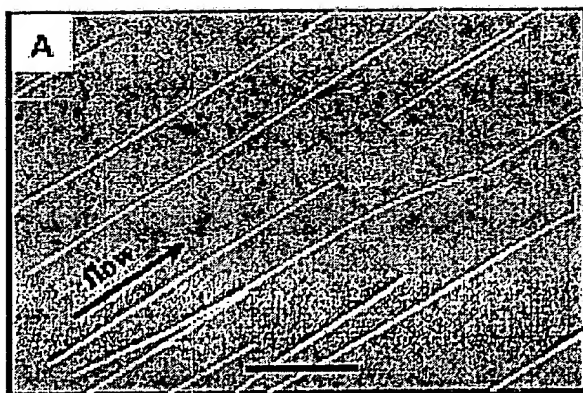


FIG. 31A

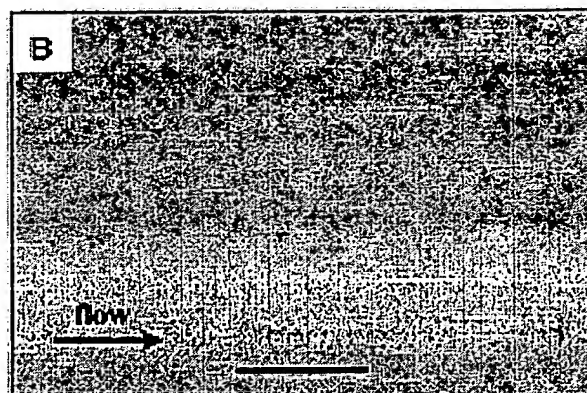


FIG. 31B

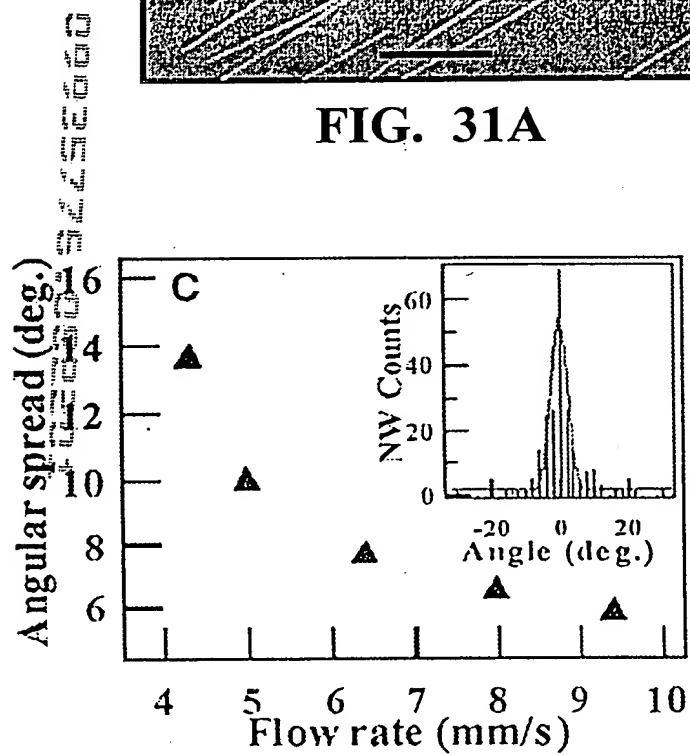


FIG. 31C

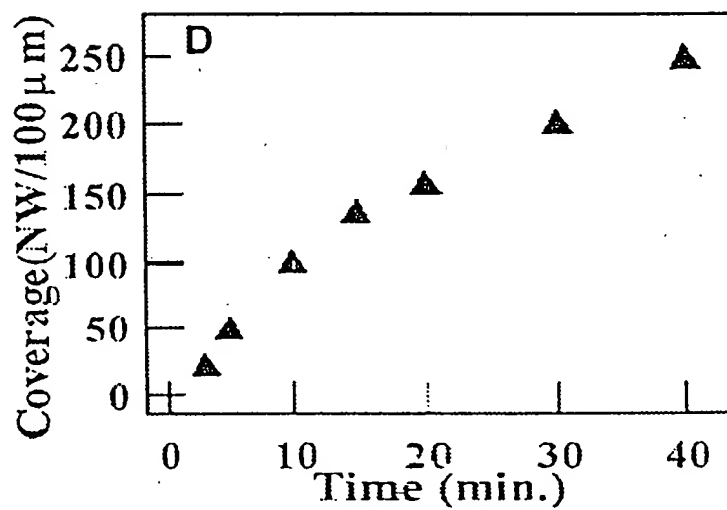


FIG. 31D

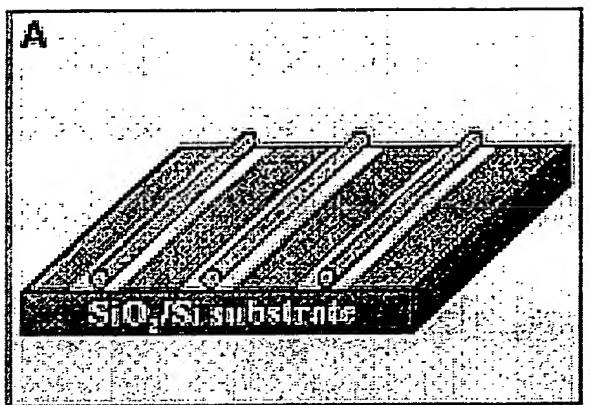


FIG. 32A

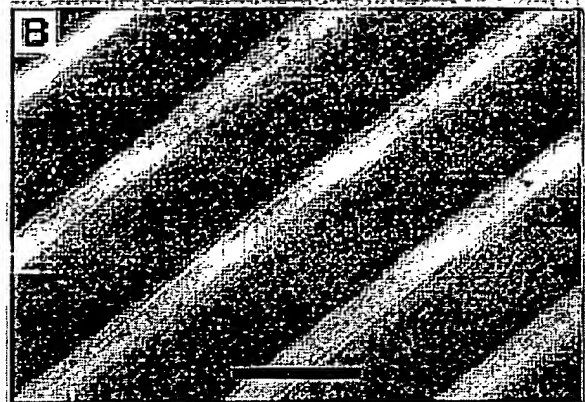


FIG. 32B



FIG. 32C

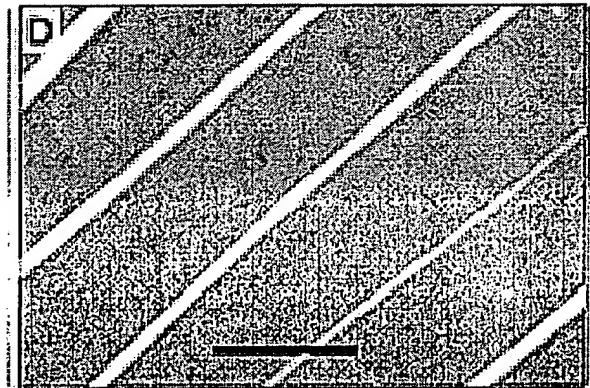


FIG. 32D

FOOTNOTES: 1000000

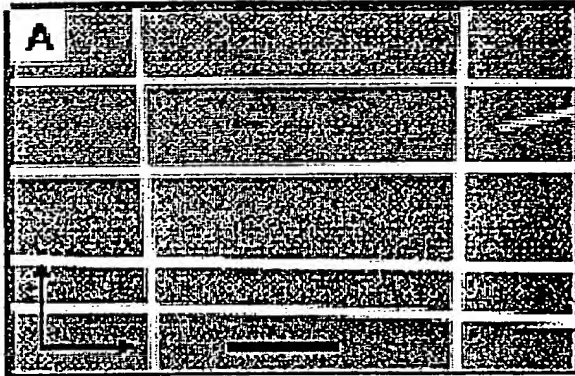


FIG. 33A

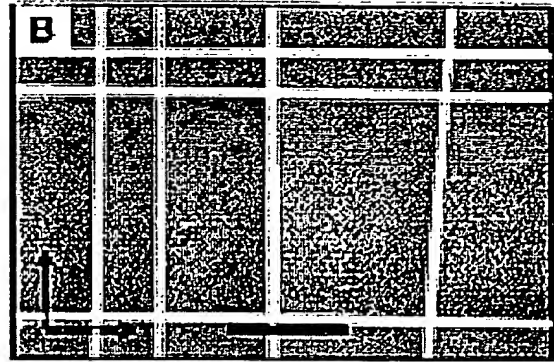


FIG. 33B

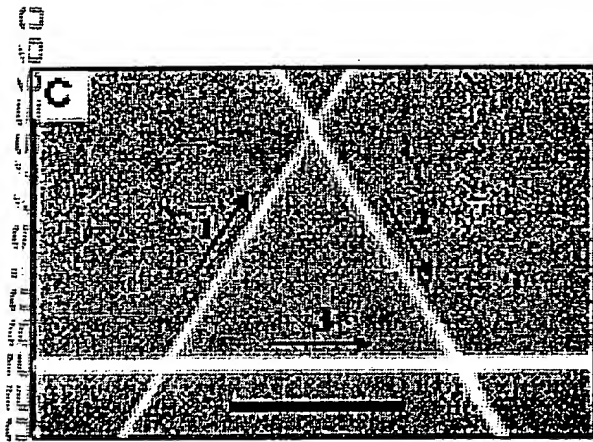


FIG. 33C

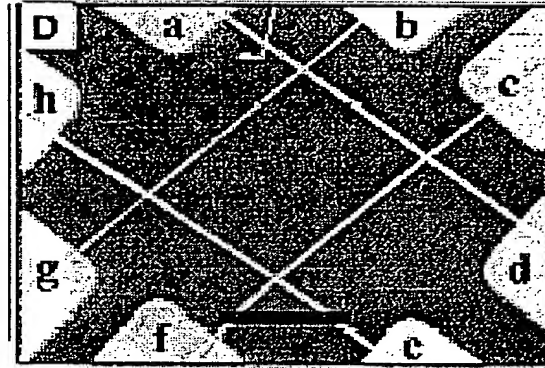


FIG. 33D

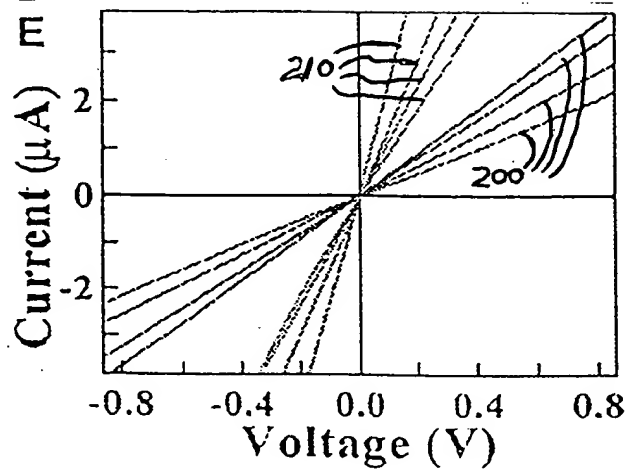


FIG. 33E